What is claimed is:

1. A semiconductor integrated circuit, comprising:

a plurality of banks, each having a plurality of memory cells, and capable of writing and reading n bits of data (where n is a positive integer) to and from the plurality of memory cells;

a plurality of input/output means, each capable of receiving a plurality of bits of data from an external circuit and outputting a plurality of bits of data to the external circuit;

an n/2-bit data bus, extending along the plurality of banks;

n bits of first data line pairs, each first data line pair being associated with each bank to transmit data between the associated bank and the data bus;

n/2 bits of second data line pairs, each second data line pair being associated with each first data line pair and each input/output means to transmit data between the data bus and the associated input/output means; and,

a plurality of switching means for connecting one of the banks with a predetermined one of the input/output means via the associated first data line pair and associated second data line pair, and with the other input/output means via the associated first data line pair, data bus and other second data line pairs, based on a control signal.

2. The semiconductor integrated circuit according to Claim 1, wherein an input buffer to input data and an output

buffer to output data are provided within each of the banks, and the input buffer and the output buffer are connected to the first data line pairs.

3. The semiconductor integrated circuit according to Claim 1, wherein each of the input/output means includes an input/output interface circuit having a plurality of input/output terminals.

4. A semiconductor integrated circuit, comprising:

a plurality of banks, each having a plurality of memory cells, and capable of writing and reading n bits of data (where n is a positive integer) to and from the plurality of memory cells;

a plurality of input/output means, positioned opposing the plurality of banks respectively, each input/output means capable of receiving a plurality of bits of data from an external circuit and of outputting a plurality of bits of data to the external circuit;

an n/2-bit data bus, extending along the plurality of banks between the plurality of banks and the plurality of input/output means;

a plurality of first data line pairs of n bits each, each first data line pair being associated with each input/output means and each bank, and extending between the associated bank and the data bus to transmits data between the associated bank and the data bus;

a plurality of second data line pairs of n/2 bits each, each second data line pair being associated with each first

data line pair and each input/output means, and extending between the data bus and the associated input/output means to transmit data between the data bus and the associated input/output means; and,

a plurality of switching means, provided at connection sites of the first data line pairs and the second data line pairs with the data bus, for connecting one of the banks with a predetermined one of the input/output means via the associated first data line pair and associated second data line pair and with the other input/output means via the associated first data line pair, data bus and other second data line pairs, based on a control signal.

5. The semiconductor integrated circuit according to Claim 4, wherein an input buffer to input data and an output buffer to output data are provided within each of the banks, and the input buffer and the output buffer are connected to the first data line pairs.

6. The semiconductor integrated circuit according to Claim 5, wherein each of the input/output means includes an input/output interface circuit having a plurality of input/output terminals.

7. A semiconductor integrated circuit, comprising:

a plurality of first banks, each having a plurality of first memory cells, and capable of writing and reading n bits of data (where n is a positive integer) to and from the plurality of first memory cells;

a plurality of second banks, positioned opposing the plurality of first banks respectively, each second bank having a plurality of second memory cells, and capable of writing and reading n bits of data to and from the plurality of second memory cells;

first and second groups of input/output means, positioned between the plurality of first banks and the plurality of second banks, the first group of input/output means being associated with the plurality of first banks respectively, the second group of input/output means being associated with the plurality of second banks respectively, each input/output means capable of receiving a plurality of bits of data from an external circuit and of outputting a plurality of bits of data to the external circuit;

a first n/2-bit data bus, extending between one of the first banks and the associated input/output means thereof, and further extending to between one of the second banks and the associated input/output means thereof;

a second n/2-bit data bus, extending between another one of the second banks and the associated input/output means thereof, and further extending to between another one of the first banks and the associated input/output means thereof such that the second n/2-bit data bus intersects the first n/2-bit data bus;

first and second groups of first data line pairs of n bits each, the first group of first data line pairs extending between the one of the first banks and the first n/2-bit data

bus to transmit data therebetween, and extending between the one of the second banks and the first n/2-bit data bus to transmit data therebetween, the second group of first data line pairs extending between the another one of the second banks and the second n/2-bit data bus to transmit data therebetween and extending between the another one of the first banks and the second n/2-bit data bus to transmit data therebetween;

first and second groups of second data line pairs of n/2 bits each, the first group of second data line pair extending between the input/output means associated with the one of the first banks and the first n/2-bit data bus to transmit data therebetween, and extending between the input/output means associated with the one of the second banks and the first n/2-bit data bus to transmit data therebetween, the second group of second data line pairs extending between the input/output means associated with the another one of the second banks and the second n/2-bit data bus to transmit data therebetween and extending between the input/output means associated with the another one of the first banks and the second n/2-bit data bus to transmit data therebetween; and,

first and second groups of switching means, the first group of switching means provided at connection sites of the first data line pairs of the first group and the second data line pairs of the first group with the first n/2-bit data bus, the second group of switching means provided at connection sites of the first data line pairs of the second group and the

second data line pairs of the second group with the second n/2-bit data bus, for connecting the one of the first banks to the associated input/output means via the associated first data line pair and second data line pair, and to other input/output means via the associated first data line pair, first n/2-bit data bus and the second data line pairs associated with the other input/output means, based on a control signal.

8. The semiconductor integrated circuit according to Claim 7, wherein an input buffer to input data and an output buffer to output data are provided within each of the banks, and the input buffer and the output buffer are connected to the first data line pairs.

9. The semiconductor integrated circuit according to Claim 8, wherein each of the input/output means includes an input/output interface circuit having a plurality of input/output terminals.